CLAIMS

Having thus described my invention, what I claim as new and desire to secure by Letters Patent is as follows:

1. A semiconductor integrated circuit having array transistors in memory cells and logic transistors wherein said array transistors have a spacing of the minimum feature size, F, said memory cells having an area of $12F^2$ or less and said logic transistors having an effective channel length of 0.7F or less, an effective gate dielectric thickness of twenty Angstroms or less, a dual work function semiconductor gate with maximum depletion thickness of 1.5 Angstroms of equivalent oxide thickness in the inversion mode and a source drain contact resistance of 3×10^{-8} or less.

2. A semiconductor integrated circuit including

array transistors having metal gate conductors encapsulated by a diffusion barrier including a thick cap insulator and a borderless source/drain contact at a spacer adjacent said thick cap insulator, and

logic transistors having silicided contacts, extension implants and a dual work function semiconductor gate having an impurity concentration of greater than 4×10^{20}.

3. A semiconductor integrated circuit as recited in claim 2, wherein said array transistors are separated by a minimum lithographic feature size.

4. A method of making an integrated circuit including steps of

forming a dielectric layer on a semiconductor substrate, said dielectric layer including a gate dielectric region,

forming a polysilicon layer on said dielectric layer and said gate dielectric region,

removing said polysilicon layer in an array area of said integrated circuit,

forming a plurality of layers including an insulator material layer on a remaining portion of said polysilicon layer and on portions of said gate dielectric such that recesses remain where polysilicon has been removed in said removing step,

forming a mask in said recesses,

removing said plurality of layers and said mask to a surface of said polysilicon,

patterning said polysilicon and a remaining portion of said plurality of layers, and

completing said integrated circuit.

5. A method as recited in claim 4, including a further step of

planarizing said dielectric layer.

6. A method as recited in claim 5, wherein said planarizing step is performed by polishing.

7. A method as recited in claim 4, wherein said plurality of layers includes a diffusion barrier and a metal conductor layer and said step of patterning forms discrete conductors.

8. A method as recited in claim 7 including the further steps of

placing mask material between portions of said polysilicon material patterned by said patterning step,

implanting impurities into said polysilicon in accordance with said mask material.

9. A method as recited in claim 8, including the further steps of

forming a silicide on a surface of said portions of said polysilicon material while preventing formation of a silicide from said discrete conductors.

10. A method as recited in claim 7, including the further step of

oxidizing surfaces of said patterned polysilicon.

11. A method as recited in claim 10, including the further step of

removing oxide on sides of said patterned polysilicon formed by said oxidizing step.

12. A method as recited in claim 11, including the further step of

forming a sidewall on sides of said patterned silicon where said oxide has been removed.

13. A method as recited in claim 10, including the further step of

forming a sidewall over a portion of said oxide formed by said oxidizing step.

14. A method as recited in claim 4, wherein said step of forming a mask includes application of a spin-on material.

15. A method as recited in claim 14, including the further step of planarizing said spin-on material.